MULTIMEDIA UNIVERSITY

STUDENT ID NO

Table Number	

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2019/2020

TSN1101 –COMPUTER ARCHITECTURE AND ORGANIZATION

(All sections / Groups)

28 Feb 2020
9.00 am – 11.00 am
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 11 pages including cover page with 4 Questions only.
2. Attempt **ALL** the **FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please print all your answers in this booklet.

QUESTION 1

a) Convert the Binary number 11100.101111_2 into the following number systems:

i) Octal
ii) Hexadecimal

[1.5 ×2 = 3 marks]

b)

i) What is the Gray code (4 bits) for decimal value 9_{10}? [2 marks]

ii) What is the advantage of Gray code over straight binary sequence? [1 mark]

Continued ...

c) Change the function F from Sum of Products (SOP) to Product of Sums (POS) form. (Show the steps involved).

$$F = ABC + \bar{A}BC + A\bar{B}C + \bar{A}\bar{B}\,C$$

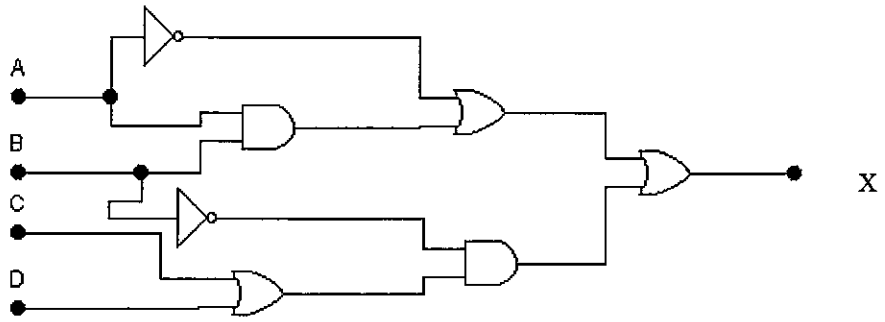
[3 marks]

d) List down 3 advantages of Digital over Analog.

[3 marks]

Continued ...

e) Find out the Boolean expression X from the circuit diagram below. [3 marks]



QUESTION 2

a)
i) Use Boolean algebra techniques to simplify the expression given below
ii) Construct the logic circuit diagram from the simplified expression obtained in (i)

$$Z = \overline{A}\,\overline{B}C\overline{D} + A\overline{B}\,CD + A\overline{B}C\overline{D}$$

[2+1 = 3 marks]

Continued ...

b) In computer science, floating-point numbers are represented by IEEE 754-32 bit single-precision format (as given below).

Sign	Biased exponent	Mantissa / Significand
1 bit	8 bits	23 bits

For the given positive 58_{10} in decimal number
i) Convert the decimal code to 8 bits unsigned binary number.
ii) Identify the normalized form of the 8 bits unsigned binary number.
iii) Identify the 8-bit biased exponent.
iv) Provide 58_{10} in IEEE 754-32 bit single-precision format

[1x 4 = 4 marks]

c)
i) Design a 3-bit parallel adder by using three full adders, where carry outputs are represented by C_1, C_2, C_3, and sum of each bit adder is represented by $\sum_1$, $\sum_2$ and $\sum_3$.

[2 marks]

Continued ...

ii) By referring to the 3-bit parallel adder in 2c (i), what is the result for C_1, C_2, C_3 and sum of each bit adder $\sum_1$, $\sum_2$, $\sum_3$ when 111_2 and 101_2 are added together.

[2 marks]

d) Design a synchronous counter that has two negative-edged triggered JK flip-flops and three inputs X, Y and Z. The counter based on the two conditions listed below:

- If X is 0, Y and Z will count up based on the present state of Z and Y.
- If X is 1, Y and Z will count down based on the present state of Z and Y.

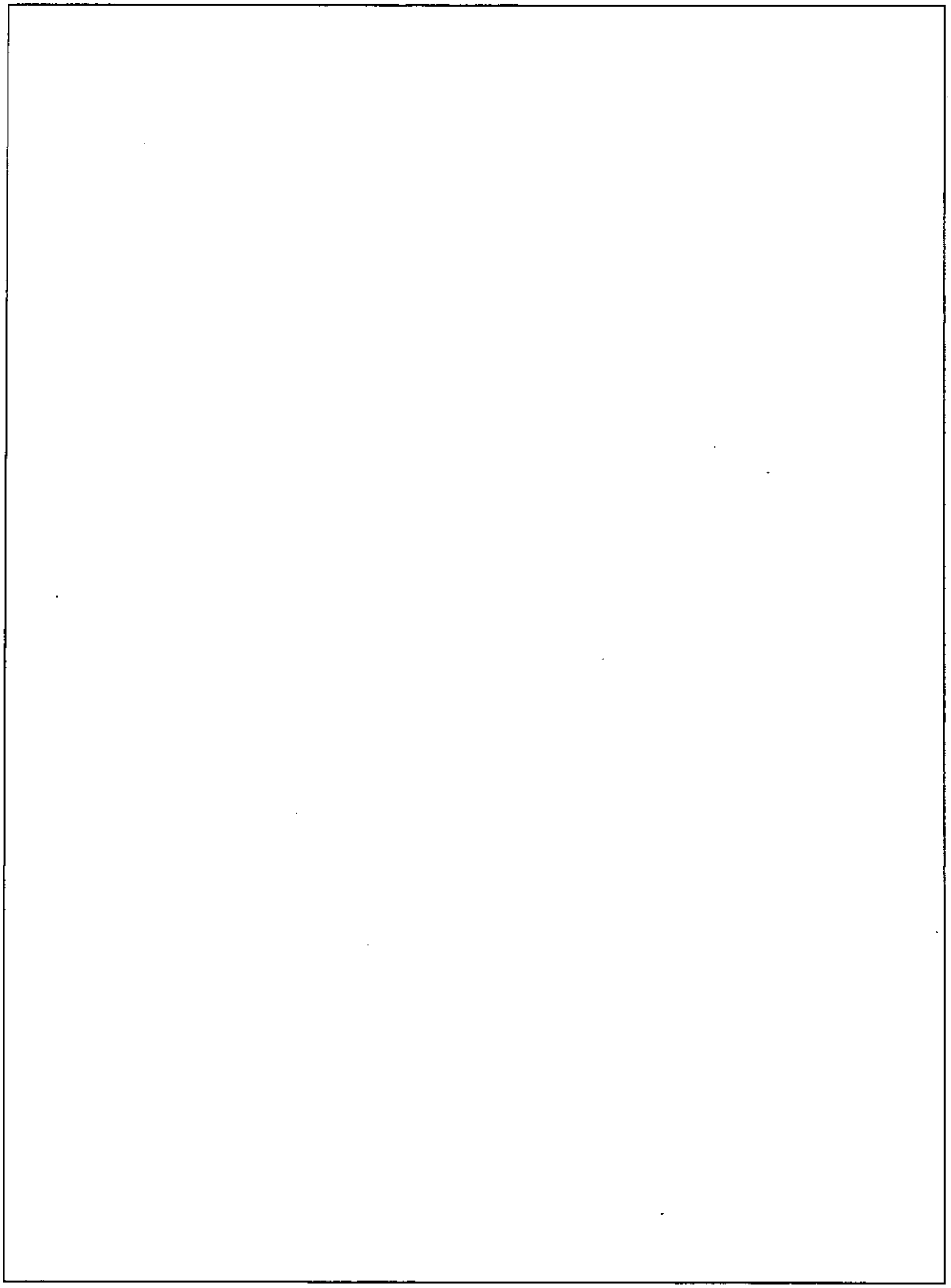
Your design should include:

(i) State Transition Diagram showing all possible states [1 mark]

(ii) By referring to Excitation Table for J-K flip flop, construct Circuit Excitation Table [2 marks]

(iii) Perform Karnaugh Map simplification for each of negative-edged triggered JK flip-flops inputs. [1 mark]

Continued ...



Continued ...

QUESTION 3

a) Contemporary computer designs are based on concepts developed by John von Neumann at the Institute for Advanced Studies, Princeton. Describe the three key concepts from John von Neumann architecture. [3 marks]

b) Within the processor there is a set of registers (user visible registers and control & status registers) that function as a level of memory above main memory and cache in the hierarchy. Describe the roles of

i) user visible registers
ii) control & status registers. [3 marks]

c) Assume that a processor employs a memory address register (MAR), a memory buffer register (MBR), a program counter (PC), and an instruction register (IR), supporting only one-address instructions. List the symbolic sequence of micro-operations for a fetch cycle. [3 marks]

Continued ...

d) Assume there is a **five-stages** instruction pipeline - Fetch (F), Decode (D), Fetch Operand (FO), Execute (E) and Write (W) running in a microprocessor. Assume that each stage requires one-time unit and no branch instruction is involved.

i. By using formula, how many time units are needed to complete these **FOUR** instructions with pipelining?
ii. By using formula, calculate the total time required to execute **FOUR** instructions without pipelining.
iii. Calculate the speedup factor for the same number of instructions.

[4 marks]

e) Assume that Word 10 contains 20, Word 20 contains 40, Word 30 contains 60, and Word 40 contains 80. Given the memory values above and a one-address machine with an Accumulator (Register A), what values do the following instructions load into the Accumulator?

i) LOAD IMMEDIATE 20
ii) LOAD DIRECT 20
iii) LOAD INDIRECT 20
iv) LOAD IMMEDIATE 40

[2 marks]

Continued ...

QUESTION 4

a) Write a program to evaluate the arithmetic expression A = [(B+C) - D)] / E, using one address instructions, two address instructions and three address instructions. The instructions available for use are as follows:

One address	Two address	Three address
LOAD X	MOVE X ,Y	
STORE X	ADD X, Y	ADD X,Y,Z
ADD X	SUB X, Y	SUB X,Y,Z
SUB X	MUL X ,Y	MUL X,Y, Z
MUL X	DIV X, Y	DIV X, Y, Z
DIV X		

[2 x 3 = 6 marks]

b) Write ARM instructions to subtract the value in memory addresses 0x2000 from the value in memory addresses 0x1000 and store the result in memory addresses 0x3000. (Hint: subtract B from A = A - B). [4 marks]

Continued ...

c) Suppose an 8-bit data word stored in memory is 1111 1000. Using the Hamming algorithm, determine what is the value of the four check bits (Check bit 8, Check bit 4, Check bit 2 and Check bit 1) that would be stored in memory with the data word. Show how you got your answer.

(4 marks)

d) Briefly explain why Direct memory access (DMA) is the best technique for Input / Output (I/O) operations. [1 mark]

End of paper